IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Amr M. Mohsen
Assignee:	Aptix Corporation
Title:	FIELD PROGRAMMABLE PRINTED CIRCUIT BOARD

Continuation of Appl'n No. 08/632,298 Filed 12 April 1996

Appl'n No:	Unknown	Filed:	Herewith
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Docket No.:	M-1007-9C US		

San Jose, California
January 17, 2002

BOX: PATENT APPLICATION
COMMISSIONER FOR PATENTS
Washington, D. C. 20231

PRELIMINARY AMENDMENT

Sir:

Please amend the above patent application as follows:

IN THE SPECIFICATION

Page 1, line 4, as a new paragraph with a heading extending to the left margin, insert

--CROSS REFERENCE TO RELATED APPLICATIONS

This is a continuation of U.S. patent application 08/632,298, filed 12 April 1996, which is a continuation of U.S. patent application 08/171,992, filed 22 December 1993, now U.S. Patent 5,544,069, which is a continuation of U.S. patent application 07/410,194, filed 20 September 1989, now U.S. Patent 5,377,124.--

Enclosed is a copy of specification page 1 in which the change to the foregoing page is indicated in red.

IN THE CLAIMS

Cancel Claims 1 - 22 without prejudice.

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Add new Claims 23 - 58 as follows:

--23. Structure comprising:

a board suitable for carrying electrically conductive traces;

a plurality of component contacts formed over said board for receipt of electronic components;

a plurality of electrically conductive traces formed over said board, each of said conductive traces being electrically connected to a corresponding one of said component contacts;

at least one programmable integrated circuit connected to said board and containing a plurality of electrically conductive leads, each of said conductive leads being electrically connected to a corresponding one of said conductive traces thereby to form an electrically conductive path from each component contact to the corresponding conductive lead, said at least one programmable integrated circuit being programmable to selectively interconnect said conductive traces through said conductive leads to achieve a desired electrical function from the electronic components to be connected to said board; and

at least one bus for transmitting information between a computer and said at least one programmable integrated circuit.

24. Structure as in Claim 23 wherein said component contacts and said conductive traces on said board have a standard configuration independent of the electronic components to be connected to said board and the electrical function to be implemented by said electronic components when selectively interconnected by said at least one programmable integrated circuit.

25. Structure as in Claim 23 wherein said board contains more than one layer of said conductive traces.

26. Structure as in Claim 23 wherein said at least one bus transmits information for exercising circuitry provided over said board.

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27. Structure as in Claim 23 wherein said at least one bus transmits information for testing circuitry provided over said board.

28. Structure as in Claim 23 wherein said at least one bus transmits information for programming said at least one programmable integrated circuit.

29. Structure as in Claim 28 wherein said at least one bus transmits information for exercising circuitry provided over said board, thereby allowing said circuitry to be exercised during programming of said at least one programmable integrated circuit.

30. Structure as in Claim 28 wherein said at least one bus transmits information for testing circuitry provided over said board, thereby allowing said circuitry to be tested during programming of said at least one programmable integrated circuit.

31. Structure comprising:

a substrate;

a plurality of component contacts formed over said substrate for receipt of electronic components;

a plurality of electrically conductive traces formed over said substrate, each of said conductive traces being electrically connected to a corresponding one of said component contacts; and

at least one programmable integrated circuit connected to said substrate and containing a plurality of electrically conductive leads, said at least one programmable integrated circuit being programmable to selectively interconnect said conductive traces through said conductive leads to achieve a desired electrical function from the electronic components to be connected to said substrate;

wherein said component contacts and said conductive traces on said substrate have a standard configuration independent of the electronic components to be mounted on said substrate and the electrical function to be implemented by said electronic components when selectively interconnected by said at least one programmable integrated circuit.

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32. Structure in Claim 31 wherein said substrate contains more than one layer of said conductive traces.

33. A method comprising:

providing input signals from a computer to at least one programmable integrated circuit which (a) is connected to a substrate, (b) contains a plurality of electrically conductive leads each connected by way of a corresponding one of a plurality of electrically conductive traces formed over said substrate to a corresponding one of a plurality of component contacts formed over said substrate for receipt of electronic components, and (c) is programmable for selectively interconnecting said conductive leads in order to programmably interconnect said electronic components to achieve a desired electrical function; and

providing output signals from said at least one programmable integrated circuit to said computer.

34. A method as in Claim 33 wherein said component contacts and said conductive traces are arranged in a standard configuration independent of said electronic components.

35. A method as in Claim 33 wherein said input and output signals carry information for exercising circuitry provided over said substrate.

36. A method as in Claim 33 wherein said input and output signals comprise test signals for testing circuitry provided over said substrate.

37. A method as in Claim 33 wherein said input and output signals comprise programming signals for controlling the selective interconnection of said conductive leads during programming of said at least programmable integrated circuit.

38. A method as in Claim 37 wherein said input and output signals include test signals for testing circuitry provided over said substrate.

39. A method as in Claim 33 wherein said substrate comprises a board suitable for carrying electrically conductive traces.

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40. A method comprising:

providing programming signals from a computer to at least one programmable integrated circuit connected to a substrate for controlling selective interconnection of a plurality of electrically conductive leads of said at least one programmable integrated circuit, each of said conductive leads being connected by way of a corresponding one of a plurality of electrically conductive traces formed over said substrate to a corresponding one of a plurality of component contacts formed over said substrate for receipt of electronic components such that the electronic components are programmably interconnected to achieve a desired electrical function; and

furnishing test signals from said computer to said at least one programmable integrated circuit to test circuitry provided over said substrate.

41. A method as in Claim 40 further including furnishing status signals from said at least one programmable integrated circuit to said computer.

42. A method as in Claim 41 further including controllably activating buffer circuitry contained in said at least one programmable integrated circuit to allow either said test signals or said status signals to pass through said buffer circuitry.

43. A method as in Claim 40 wherein said substrate comprises a board suitable for carrying electrically conductive traces.

44. Structure comprising:

a board suitable for carrying electrically conductive traces;

a plurality of component contacts formed over said board for receipt of electronic components;

a plurality of electrically conductive traces formed over said board, each of said conductive traces being electrically connected to a corresponding one of said component contacts;

at least one programmable integrated circuit connected to said board and containing a plurality of electrically conductive leads, each of said conductive leads being electrically connected to a corresponding one of said conductive traces thereby to form an

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electrically connected to a corresponding one of said conductive traces thereby to form an electrically conductive path from each component contact to the corresponding conductive lead, said at least one programmable integrated circuit being programmable to selectively interconnect said conductive traces to achieve a desired electrical function from the electronic components to be connected to said board; and

at least one bus for transmitting information between a computer and circuitry provided over said board.

45. Structure as in Claim 44 wherein said component contacts and said conductive traces on said boards are arranged in a standard configuration independent of the electronic components to be connected to said board and the electrical function to be implemented by said electronic components when selectively interconnected by said at least one programmable integrated circuit.

46. Structure as in Claim 44 wherein said board contains more than one layer of said conductive traces.

47. Structure as in Claim 44 wherein said at least one bus transmits information for exercising circuitry provided over said board.

48. Structure as in Claim 44 wherein said at least one bus transmits information for testing circuitry provided over said board.

49. Structure as in Claim 44 wherein said at least one bus transmits information for programming said at least one programmable integrated circuit.

50. Structure as in Claim 49 wherein said at least one bus transmits information for exercising circuitry provided over said board, thereby allowing said circuitry to be exercised during programming of said at least one programmable integrated circuit.

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51 52. A method comprising:

providing input signals from a computer to circuitry provided over a substrate connected to at least one programmable integrated circuit which (a) contains a plurality of electrically conductive leads each connected by way of a corresponding one of a plurality of electrically conductive traces formed over said substrate to a corresponding one of a plurality of component contacts provided over said substrate for receiving electronic components and (b) is programmable for selectively interconnecting said conductive leads in order to programmably interconnect said electronic components to achieve a desired electrical function; and

providing output signals from circuitry provided over said substrate to said computer.

52 53. A method as in Claim 52 wherein said component contacts and said conductive traces are arranged in a standard configuration independent of said electronic components.

53 54. A method as in Claim 52 wherein said input and output signals carry information for exercising circuitry provided over said substrate.

54 55. A method as in Claim 52 wherein said input and output signals comprise test signals for testing circuitry provided over said substrate.

55 56. A method as in Claim 52 wherein said input and output signals comprise programming signals for controlling the selective interconnection of said conductive leads during programming of said at least programmable integrated circuit.

56 57. A method as in Claim 56 wherein said input and output signals include test signals for testing circuitry provided over said substrate.

57 58. A method as in Claim 52 wherein said substrate comprises a board suitable for carrying electrically conductive traces.--

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REMARKS

The specification has been amended to recite the priority information.

All of original Claims 1 - 22 have been canceled. Claims 23 - 58 have been added. Accordingly, Claims 23 - 58 are now pending.

Claims 23 - 58 substantially respectively repeat canceled Claims 29 - 36, 40, 41, 43 - 49, and 53 - 71 of parent U.S. patent application 08/632,298.

Please telephone Applicant's attorney at 408-453-9200, ext. 1371, if there are any questions.

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Respectfully submitted,

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FIELD PROGRAMMABLE PRINTED CIRCUIT BOARD

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FIELD OF THE INVENTION

This invention relates to printed circuit boards and in particular to a printed circuit board which is programmable in the field by the designer of an electronic system to provide a desired function and to the method of programming the programmable printed circuit board of this invention.

BACKGROUND OF THE INVENTION

Printed circuit boards are commonly used in electronic devices such as instruments, computers, telecommunication equipment and consumer electronic products. Typically, an engineer will design a printed circuit board to carry the types of components necessary to implement the desired electronic function and to fit in the space available for the board. Consequently, each printed circuit board typically is custom designed. To design a custom printed circuit board is expensive, takes time and requires the fabrication of prototype printed circuit boards. If errors are found in the prototypes, then the printed circuit board must be redesigned. Such a process often delays the planned introduction of a new product.

SUMMARY OF THE INVENTION

In accordance with this invention, a printed circuit board of unique configuration is combined with one or more special programmable integrated circuit chips (hereinafter called "programmable interconnect chips" or "PICs") to provide a user programmable printed circuit board capable of being used to provide any one of a plurality of functions.

In one embodiment of the invention, a field programmable printed circuit board comprises

(1) a multiplicity of component contacts for receipt of the leads of electronic components;

(2) a corresponding multiplicity of PIC contacts

CROSS REFERENCE TO RELATED APPLICATIONS

This is a continuation of U.S. patent - 1 - application 08/632,298, filed 12 April 1996, which is a continuation of U.S. patent application 08/171,912 filed 22 December 1993, now U.S. Patent 5,544,069, which is a continuation of U.S. patent application 07/410,194, filed 20 September 1989, now U.S. Patent 5,377,124.